Abstract

An endpoint processor includes a processor block, a timer block, a memory block, and analog-to-digital converter. The timer block is arranged to provide a time based signal to the processor block. The memory block cooperates with the processor block. The analog-to-digital converter is arranged to provide an interface between an analog signal and the processor block. The analog signal includes encoded data from a power signal. The processor block is arranged to control a sampling rate that is associated with the analog-to-digital converter such that the analog signal is down-converted as an under-sampled signal. The processor block is arranged to extract the encoded data from the down-converted signal by executing a digital signal processing algorithm that is stored in the memory block. The digital signal processing algorithm is arranged to reject fundamental and harmonic frequencies that are associated with a power-line frequency that is associated with the power signal.

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